

Development and optimization of a SYCL backend for libCEED

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Outline

- Software design of libCEED
- > SYCL online compiler
- > Optimization of hotspot kernels
 - □ Specialization constant
 - Tuning workgroup sizes/barriers
 - **SIMD** size/register width
- Summary and Future work

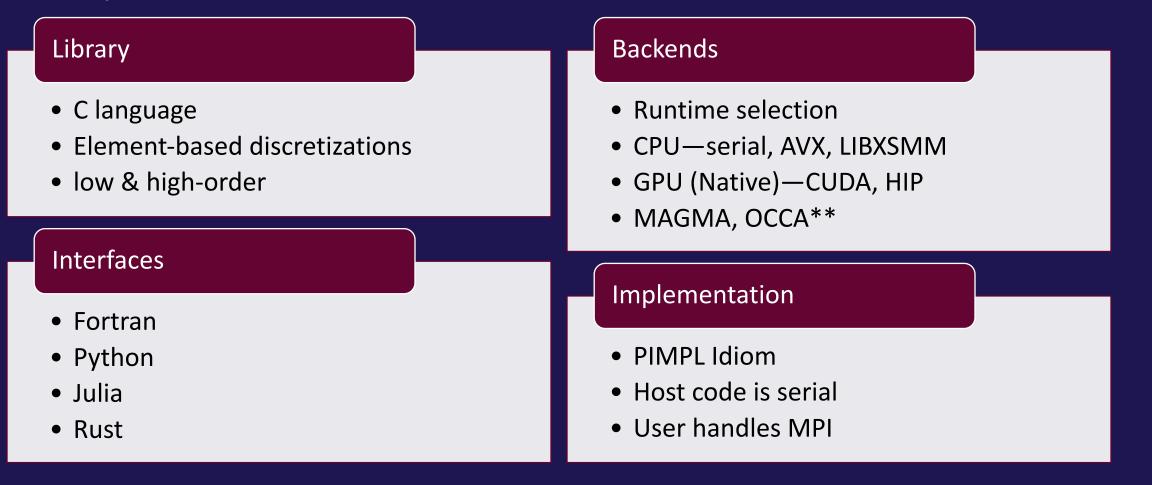
Disclaimer: This work was done on a pre-production supercomputer with early versions of the Aurora software development kit.



libCEED

Developed through CEED co-design center as part of the ECP courtesy: Jed Brown, Natalie Beams and others.

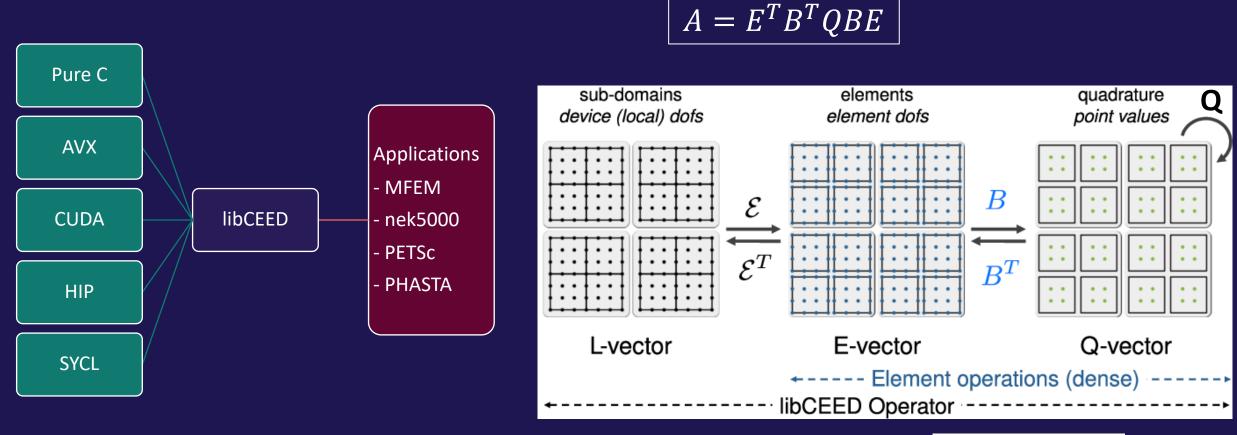
https://github.com/CEED/libCEED





Overview of libCEED operations

• Portable library that provides an API for applications to share efficient kernels for element-based discretizations.





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https://github.com/CEED/libCEED

libCEED Runtime Compilation Usage

Constants	polynomial order	
	spatial dimension	
Determine loop-bounds	element count	
	node count	
Operate pointwise at mesh nodes	Boundary conditions	
	Forces	
Injected into kernels	Problem-dependent	
	Avoids memory traffic	
	Determine loop-bounds Operate pointwise at mesh nodes	



Runtime code compilation in libCEED

- libCEED host application generates device code at runtime based on user input (the code is in stringstream) – compiles and runs on GPU devices.
- CUDA backend uses nvrtc for runtime compilation of generated kernels.
- Two possible solutions for SYCL
 - > Using specialization constant (a partial alternative)
 - > Using Intel's oneAPI online compilation extension (experimental early access) -

https://github.com/intel/llvm/blob/sycl/sycl/doc/extensions/experimental/sycl_ext_intel_online_compiler.asciidoc



Existing CUDA Backend

AOT Compilation

Online Compilation

- Uses nvcc
- Some (few) kernels
- Uses NVRTC
- Kernel source string is generated
- Boilerplate code is provided (e.g., read/writes with global mem)
- User source code is loaded from file
- Create BP→UserDefinedFunc→BP "sandwich"
- Load Cumodule, use CUfunction



Designing the SYCL Backend

Problem Parameters	Specialization constants		
	Define kernels using lambdas or functors		
	CUDA module can be replaced by SYCL kernel bundle		
User Functions	How to compile source code string? (Ideal)		
	How to link compiled user functions? (Fallback)		



libCEED SYCL Online Compilation

- The libCEED CUDA and HIP backends use their respective vendor runtime compilation libraries (e.g., nvrtc, hiprtc).
- The current SYCL spec doesn't prescribe similar functionality.
- An Intel extension for SYCL allows for the runtime compilation of OpenCL C source.
 - Provided to SYCL API as a std::string
- Restriction to OpenCL C required some workarounds when porting libCEED jit source.
 - E.g., No templates, no function pointers
 - Also required some workarounds in QFunction implementation.
- We are working with Intel compiler team to help drive the online compiler extension forward.
- Future versions may support runtime compilation of SYCL source

https://github.com/intel/llvm/blob/sycl/sycl/doc/extensions/experimental/sycl_ext_oneapi_kernel_compiler.asciidoc



Intel Online Compiler SYCL Extension

- Experimental extension
- Calls ocloc library API (libigc)
- Compile OpenCL string to "binary blob"
- How to use "binary blob"?

Alternatives are not ideal

- OpenCL plugin only + interop
- Use Level Zero + libigc directly

#include "sycl/ext/intel/online_compiler.hpp"

#include <iostream>
#include <vector>

```
static const char *kernelSource = R"===(
__kernel void my_kernel(__global int *in, __global int *out) {
    size_t i = get_global_id(0);
    out[i] = in[i] + 1;
}
)===";
Example from
```

using namespace sycl::INTEL;

```
int main(int argc, char **argv) {
    online_compiler<source_language::opencl_c> compiler;
    std::vector<byte> blob;
```

```
try {
  blob = compiler.compile(
    std::string(kernelSource),
    std::vector<std::string> {
       std::string("-cl-fast-relaxed-math")
    }
  );
}
catch (online_compile_error &e) {
   std::cout << "compilation failed\n";
   return 1;
}</pre>
```

return 0;



Intel LLVM docs

```
sycl::kernel *buildKernelFromSource(const sycl::device &sycl device,
                                                                                    const sycl::context &sycl context,
                                                                                    const std::string &kernel name,
                                                                                    const std::string &kernel source,
                                                                                    const std::vector<std::string> &flags) {
                                                   using namespace sycl::ext::intel::experimental;
                                                   online compiler<source language::opencl c> compiler(sycl device);
                                                   std::vector<unsigned char> blob;
                                                   try { blob = compiler.compile(kernel_source, flags);}
Example
                                                   catch (online compile error &e) {
                                                     std::cout << "compilation failed\n";</pre>
                                                     std::exit(EXIT_FAILURE);
Online Compiler + Level Zero
                                                   const char *lz_flags = "-ze-opt-level=2";
sycl queue.submit([&](sycl::handler &cgh)
  cgh.depends_on({copy_x, copy_y});
                                                                                  nullptr,
  cgh.set_args(alpha, x, y);
                                                                                  blob.size(),
  cgh.parallel for(N, *axpy kernel);
                                                                                  lz_flags,
});
                                                                                  nullptr};
                                                   ze module handle t lz module;
                   SYCL kernel bundle
                                                   ));
                                                   ze kernel handle t lz kernel;
                                                   auto *sycl kernel = new sycl::kernel(
                           SYCL kernel
                                                   ));
                                                   return sycl_kernel;
```

binary blob auto lz device = sycl::get native<sycl::backend::ext oneapi level zero>(sycl device); auto lz context = sycl::get native<sycl::backend::ext oneapi level zero>(sycl context); ze module desc t lz mod_desc = {ZE_STRUCTURE_TYPE_MODULE_DESC, ZE_MODULE_FORMAT_IL_SPIRV, LZ module descriptor blob.data(), LZ module zeModuleCreate(lz context, lz device, &lz mod desc, &lz module, nullptr); auto *sycl module = new sycl::kernel bundle<sycl::bundle state::executable>(sycl::make kernel bundle<sycl::backend::ext oneapi level zero,sycl::bundle state::executable>({lz module, sycl::ext::oneapi::level_zero::ownership::transfer},sycl context ze_kernel_desc_t lz_kernel_desc = {ZE_STRUCTURE_TYPE_KERNEL_DESC, nullptr, 0,kernel_name.c_str()}; LZ kernel zeKernelCreate(lz_module, &lz_kernel_desc, &lz_kernel); sycl::make kernel<sycl::backend::ext oneapi level zero>({*sycl_module, lz_kernel,sycl::ext::oneapi::level_zero::ownership::transfer},sycl_context

libCEED Implementation

using SyclModule_t = sycl::kernel_bundle<sycl::bundle_state::executable>;

int CeedJitGetKernel_Sycl(Ceed ceed, const SyclModule_t *sycl_module, const std::string &kernel_name, sycl::kernel **sycl_kernel) {
 Ceed_Sycl *data;

CeedCallBackend(CeedGetData(ceed, &data));

// sycl::get_native returns std::vector<ze_module_handle_t> for lz backend
// https://github.com/intel/llvm/blob/sycl/sycl/doc/extensions/supported/sycl ext oneapi backend level zero.md

ze module handle t lz module = sycl::get native<sycl::backend::ext oneapi level zero>(*sycl module).front();

```
ze_kernel_desc_t lz_kernel_desc = {ZE_STRUCTURE_TYPE_KERNEL_DESC, nullptr, 0, kernel_name.c_str()};
ze_kernel_handle_t lz_kernel;
zeKernelCreate(lz_module, &lz_kernel_desc, &lz_kernel);
```

```
return CEED_ERROR_SUCCESS;
```



SYCL queue synchronization for external libraries

- Streams in CUDA and HIP are in-order.
- A global default stream is available simplifying the coordination with external libraries.
- Initial implementation of SYCL backends used in-order queues.
- CEED-PHASTA uses PETSc
 - For Intel GPUs, PETSc uses Kokkos-SYCL backend
 - Kokkos-SYCL uses out-of-order SYCL queues
- For synchronization with PETSc, libCEED SYCL inputs SYCL queue from PETSc.
- To use out-of-order queues with the libCEED SYCL implementation, the Intel SYCL extension for enqueueing (asynchronous, device-side) enqueue barriers were used.
- Future development will look to use SYCL events to explicitly express data dependencies within libCEED.



Performance Baseline

- sycl-fluids examples using Blasius test case.
 - Overall time per iteration on A100 was 3.7 sec
 - Overall time per iteration on PVC was 70 seconds
- 3 hotspots identified for both A100 and PVC.
 - CeedBasisSyclGrad SYCL kernel
 - CeedBasisSycIInterp SYCL kernel
 - IJacobian (OpenCL kernel which is online compiled)

Kernel	PVC (1 Tile)	A100 (CUDA)
IJacobian	29 ms	0.92 ms
Interp	10.7 ms	0.11 ms
Grad	197 ms	1.3 ms



BASIS GRAD KERNEL

Using microbenchmarks of the kernel

	#define CeedScalar float	26	int CeedBasisGrad_Sycl(sycl::queue &sycl_queue, CeedBasis_Sycl *impl, CeedScalar *u, CeedScalar *v) {
	#define NTRIALS 1001	27	
9		28	const CeedInt dim = impl->dim; const CeedInt Q_1d = impl->Q_1d; Kernel in function
	class CeedBasisSyclGrad;	29	<pre>const CeedScalar *grad_1d = impl->d_grad_1d;</pre>
11		30	
	Inc main() (31	<pre>const CeedInt work_group_size = 32;</pre>
13	// Secup Options	32	<pre>sycl::range<1> local_range(work_group_size);</pre>
14	const Ceedint U la = 2;	33	<pre>sycl::range<1> global_range(num_elem * work_group_size);</pre>
15	const (codint num olom = 10% 90% 141.	34 35	<pre>sycl::nd_range<1> kernel_range(global_range, local_range);</pre>
16	const CoodInt dim = 2.	35 36	<pre>sycl queue.submit([&](sycl::handler &cgh) {</pre>
17		37	<pre>syc1_queue.submit([a](syc1::nandier &cgn) { syc1::local accessor<ceedscalar> s mem(2 * (P * Q + buf len), cgh);</ceedscalar></pre>
18		38	cgh.parallel for <ceedbasissyclgrad>(kernel range, [=](sycl::nd item<1> work item) {</ceedbasissyclgrad>
19		39	
20		40	<pre>});</pre>
21	// ···································	41	<pre>});</pre>
22	<pre>sycl::range<1> global range(num elem * work group size);</pre>	42	return 1;
23	sycl::nd range<1> kernel range(global range, local range):	43	}
24		44	
25	float walltimer[NUPTAIS] awa time:		<pre>int main() {</pre>
26	for the trial of the later of t	46	// Setup options
20		47	const CeedInt Q_1d = 2;
28		48 49	const CeedInt dim = 3;
28 29		49 50	// SYCL initialization
29 30		50 51	// SIGE INICIALIZACION
	γ	51	// Ceed Basis setup
31		5.2	CeedBasis Secup CeedBasis Sycl *basis = (CeedBasis Sycl*)calloc(1,sizeof(CeedBasis Sycl));
32	E CONTRATATIET TORSCEEDBASISSVCIGRADZIKERNET RANDE, I-LUSVCIIING TLEMSTZ WORK TLE	54	basis->dim = dim;
33		55	<pre>basis->Q_1d = Q_1d;</pre>
34		56	<pre>basis->d_grad_1d = sycl::malloc_device<ceedscalar>(interp_length, sycl_device, sycl_context);</ceedscalar></pre>
35		57	
36		58	<pre>for(int trial=0;trial<ntrials;trial++) pre="" {<=""></ntrials;trial++)></pre>
37		59	<pre>auto start_time = std::chrono::high_resolution_clock::now();</pre>
38		60	<pre>result = CeedBasisGrad_Sycl(sycl_queue, basis, d_u, d_v);</pre>
39		61	<pre>sycl_queue.wait_and_throw();</pre>
10	walltimes[tilal] - stuthtohouulation(libat, stuhttl)/(lihish time stalt time	62	the finish him - shitted and high an obtain -lash and ()
11		63 64	<pre>auto finish_time = std::chrono::high_resolution_clock::now(); walltimes[trial] = std::chrono::duration<float,std::milli>(finish time-start time).count();</float,std::milli></pre>
12		64 65	<pre>walltimes[trial] = stu::chrono::duration(itoat,stu::milli>(linisn_time-start_time).count(); </pre>
		05	
	15 Arganna Loadarshin Computing Facility		Kernel execution time = 5.8 ms Argonne 🐴

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Kernel execution time = 5.8 ms



Use of SYCL specialization constants

```
12
     using SpecID = sycl::specialization id<CeedInt>;
13
    using SyclModule t = sycl::kernel bundle<sycl::bundle state::executable>;
14
15
     static constexpr SpecID BASIS Q 1D ID;
16
     static constexpr SpecID BASIS DIM ID;
17
18
    int CeedBasisGrad Sycl (sycl::queue &sycl queue, const SyclModule t& sycl module, CeedBasis Sycl *impl, const CeedScalar *u, CeedScalar *v) {
19
       sycl::range<1>
                          local range (work group size);
20
                          global range(num elem * work group size);
      sycl::range<1>
       sycl::nd range<1> kernel range(global range, local range);
21
22
23
       sycl::event e = sycl queue.ext oneapi submit barrier();
24
       sycl queue.submit([&](sycl::handler &cgh) {
25
        cqh.depends on({e});
26
         cgh.use kernel bundle(sycl module);
27
         sycl::local accessor<CeedScalar> s mem(2 * (op len + buf len), cgh);
28
29
         c<u>qh.parallel for<CeedBasisSyclGrad<transpose>>(kernel range, [=](sycl::nd item<1> work item, sycl::kernel handler kh) {</u>
          // Retrieve spec constants ----->
30
31
           const CeedInt dim
                                      = kh.get specialization constant<BASIS DIM ID>();
32
          const CeedInt Q 1d
                                      = kh.get specialization constant<BASIS Q 1D ID>();
33
34
         // Work
35
         });
36
       });
37
       return 1;
38
39
40
    int main() {
41
      // Initialization
42
43
      std::vector<sycl::kernel id> kernel ids = { sycl::get kernel id<CeedBasisSyclGrad<1>>(), sycl::get kernel id<CeedBasisSyclGrad<0>>() };
44
       sycl::kernel bundle<sycl::bundle state::input> input bundle = sycl::get kernel bundle<sycl::bundle state::input>(sycl context, kernel ids);
45
46
      input bundle.set specialization constant<BASIS DIM ID>(dim);
47
      input bundle.set specialization constant<BASIS Q 1D ID>(Q 1d);
48
       SyclModule t *sycl module = new SyclModule t(sycl::build(input bundle));
49
50
       for(int trial=0;trial<NTRIALS;trial++) {</pre>
51
         auto start time = std::chrono::high resolution clock::now();
52
         result = CeedBasisGrad Sycl<1>(sycl queue, *sycl module, num elem, basis, d interp 1d, d grad 1d, d u, d v);
53
         sycl queue.wait and throw();
54
55
         auto finish time = std::chrono::high resolution clock::now();
                                                                                      Kernel execution time = 1.38 ms
56
         walltimes[trial] = std::chrono::duration<float,std::milli>(finish time-start
57
```



Further optimizations on CeedBasisGrad

- Adjust WG size from 1024 to 32.
- Replace workgroup barrier with nd_item barrier

sycl::group_barrier(work_group) → work_item.barrier(sycl::access::fence_space::local_space)

• Remove IGC runtime memory checks by using specialization constant.

warning: from dir:/home/vmadananth/PHASTA_aesp_CNDA/CEED-PHASTA/libCEED/backends/sycl-ref from file:ceed-sycl-ref-basis.sycl.cpp line:100 :Adding additional control flow due to presence of generic address space operations warning: from dir:/home/vmadananth/PHASTA_aesp_CNDA/CEED-PHASTA/libCEED/backends/sycl-ref from file:ceed-sycl-ref-basis.sycl.cpp line:185 :Adding additional control flow due to presence of generic address space operations warning: from dir:/home/vmadananth/PHASTA_aesp_CNDA/CEED-PHASTA/libCEED/backends/sycl-ref from file:ceed-sycl-ref-basis.sycl.cpp line:187 :Adding additional control flow due to presence of generic address space operations warning: from dir:/home/vmadananth/PHASTA_aesp_CNDA/CEED-PHASTA/libCEED/backends/sycl-ref from file:ceed-sycl-ref-basis.sycl.cpp line:187 :Adding additional control flow due to presence of generic address space operations warning: from dir:/home/vmadananth/PHASTA_aesp_CNDA/CEED-PHASTA/libCEED/backends/sycl-ref from file:ceed-sycl-ref-basis.sycl.cpp line:187 :Adding additional control flow due to presence of generic address space operations warning: from dir:/home/vmadananth/PHASTA_aesp_CNDA/CEED-PHASTA/libCEED/backends/sycl-ref from file:ceed-sycl-ref-basis.sycl.cpp line:0 :Adding additional control flow due to presence of generic address space operations

Kernel	PVC (1 Tile)	A100
IJacobian	29ms	0.9ms
Interp	<mark>1.75ms</mark>	<mark>0.11ms</mark>
Grad	<mark>4.8ms</mark>	<mark>1.3ms</mark>



Optimizations performed on IJacobian

- IJacobian kernel was using default range. The compiler was setting the workgroup size to 32.
 - Changing to default nd_range and setting WG size to 384 (CUDA) improved performance slightly.
- Reducing register spills
 - Building with AOT did not show any warnings on spills as this was OpenCL kernel.
 - Inspected assembly by setting the following env variables
 - IGC_DumpToCurrentDir=1, IGC_DumpToCurrentDir=1
 - For more IGC env variables <u>https://github.com/intel/intel-graphics-compiler/blob/master/documentation/configuration_flags.md</u>
 - Generates asm for all kernels. To search for kernel names –

for f in ./*.asm; do echo "-----"; echo \$f; cat \$f | grep "\V.kernel"; done

//.kernel CeedKernelSyclRefQFunction_IJacobian_Newtonian_Prim //.platform PVCXT			
//.thread_config numGRF=128, numAcc=4, numSWSB=16			
//.options_string ""			
<pre>//.full_options "-emitLocation -forceAssignRhysicalReg "" -hasRNEandDenorm -noStitchExternFunc -linker 0 -lscEnableImmOffsFor 196638 - preserver0 -TotalGRFNum 128 -abortOnSpill 4 -boundsChecking -presched-ctrl 6 -presched-rp 100 -nodpsendreorder -SBIDDepLoc -output - binary -dumpcommonisa -shaderDumpFilter "" -dumpvisa -printHexFloatInAsm -noverifyCISA -enableHalfLSC -hasInt64Add -partialInt64 -</pre>			
generateDebugInfo "			
//.instCount 3207			
//.RA type GRAPH_COLORING_SPILL_FF_RA			
//.spill size 54784			
//.spill GRF est. ref count 1475			



Reducing spills

- By default, PVC has 128 64-byte registers allocated per thread.
- Registers spills can be expensive. Improve register usage per thread by
 - Increasing the registers available per thread to 256
 - Running in lower SIMD width
- Passing large register file with online compilation.

• Enforcing SIMD16 with OpenCL kernel

__attribute__(intel_reqd_sub_group_size(16))

https://registry.khronos.org/OpenCL/extensions/intel/cl_intel_required_subgroup_size.html



Where does performance stand currently

Kernel	A100	PVC (before optimization)	PVC (after optimizations)
IJacobian	0.9 ms	29 ms	1.1 ms
Grad	1.3 ms	6.4 ms	4.5 ms
Total time per timestep	3.6 s	70 s	11 s

*This is still a work in progress, and not a representative of performance between two hardware

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Key Takeaways

Intel online compiler SYCL extension

- Allows for NVRTC-like runtime compilation
- Currently restricted to use of OpenCL C/LevelZero kernels (interop)
- In future, likely to extend support for SYCL kernel code

Optimization Strategies

- Specialization constants useful for optimizing code with parametric values. Runtime increases with number of spec. constants
- Use of appropriate workgroup sizes and barriers.
- For register-heavy kernels large GRF + smaller SIMD width

Future Work

- Systematic profiling of online compiled code for further insights on performance bottlenecks.
- Use of the updated SYCL kernel compiler with SYCL user functions.



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